概要

AXS2045 是一款2x40W立体声D类音频放大器。可编程功率限制和放大增益。支持单端或差分输入，BTL输出可驱动4-8Ω扬声器、PBTL输出可驱动2-4Ω扬声器。

特有的高 PSRR 的反馈功率级架构，实现低噪声、低失真。自适应混合调制技术，可动态降低功率损耗，提升工作效率，有效延长电池供电音响系统的待机时间。

集成了全面的保护特性，包括短路、热关断、过压、欠压和直流扬声器保护。在过载情况下，器件会将故障情况报告给处理器，从而避免自身遭到损坏。

AXS2045 提供 ETSSOP24 封装。底部带 E-PAD 散热焊盘，无需额外的散热器。

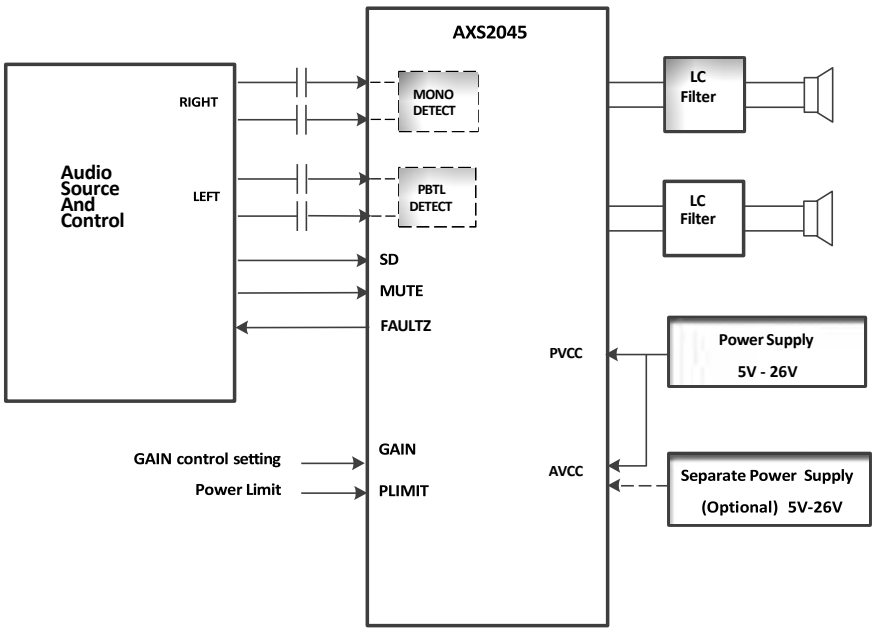
特性

- 宽电源电压范围 5V 至 26V
- 可选增益：20dB、26dB、32dB
- D类最大输出功率：
  - BTL：2x20W（4Ω、10% THD+N、12V）
  - BTL：2x40W（8Ω、10% THD+N、24V）
  - BTL：2x55W（4Ω、1% THD+N、24V）
  - PBTL：1x80W（3Ω、1% THD+N、24V）
- 开关机POP声抑制
- 工作效率：> 90%
- 超低静态电流：12mA @12V

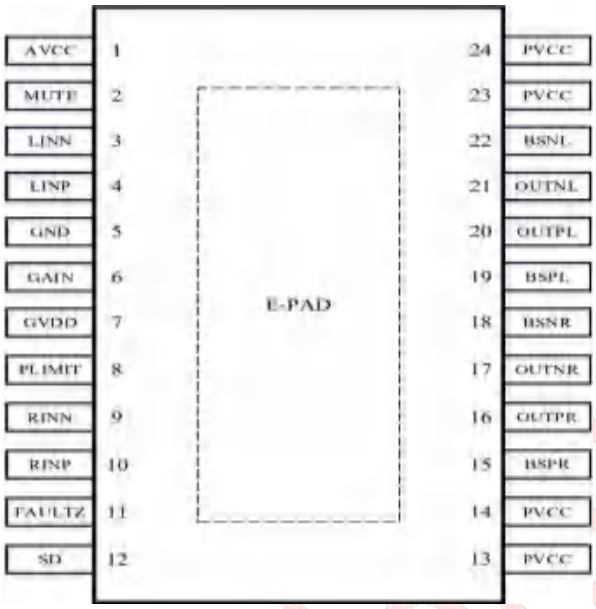
应用

- 无线音箱、智能音箱、条形音箱、直播音箱
- 电视机、投影仪、书架音箱、家庭影院

简化应用电路



Pin Configuration and Functions：



PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	AVCC	P	Analog Supply
2	MUTE	I	Mute signal for fast disable/enable of outputs (HIGH = outputs Hi-Z, LOW = outputs enabled). TTL logic levels with compliance to AVCC.
3	LINN	I	Negative audio input for left channel. Connect to GND for PBTL mode.
4	LINP	I	Positive audio input for left channel. Connect to GND for PBTL mode.
5	GND	G	Ground
6	GAIN	I	Selects Gain mode depending on pin voltage divider. Refer to: Gain Setting
7	GVDD	PO	Internally generated gate voltage supply. Not to be used as a supply or connected to any component other than a 1 µF X7R ceramic decoupling capacitor and the PLIMIT and GAIN resistor dividers. Refer to: GVDD Supply
8	PLIMIT	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit. Refer to: PLIMIT Operation
9	RINP	I	Positive audio input for right channel. Connect to GND for MONO mode.
10	RINN	I	Negative audio input for right channel. Connect to GND for MONO mode.
11	FAULTZ	DO	General fault reporting including Over-temp, DC Detect. Open drain. Refer to: Device Protection System FAULTZ = High, normal operation. FAULTZ = Low (an external 100 kΩ pull-up resistor required), fault condition
12	SD	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC. Refer to: Startup and Shutdown Operation
13,14	PVCC	P	Power supply
15	BSPR	BST	Boot strap for positive right channel output, connect to 220 nF X5R or better ceramic cap to OUTPR. Refer to: BSPx and BSNx Capacitors
16	OUTPR	PO	Positive right channel output
17	OUTNR	PO	Negative right channel output
18	BSNR	BST	Boot strap for negative right channel output, connect to 220 nF X5R, or better ceramic cap to OUTNR. Refer to: BSPx and BSNx Capacitors
19	BSPL	BST	Boot strap for positive left channel output, connect to 220 nF X5R, or better ceramic cap to OUTNL Refer to: BSPx and BSNx Capacitors
20	OUTPL	PO	Positive left channel output
21	OUTNL	PO	Negative left channel output
22	BSNL	BST	Boot strap for negative left channel output, connect to 220 nF X5R, or better ceramic cap to OUTPL
23, 24	PVCC	P	Power supply
	E-PAD	G	Connect to GND

Order Information

Part Number	Package Type	Marking	Package Qty	Temp Range (°C)
AXS2045	ETSSOP24	AXS2045 XXXXXXX XXXX	Tape and Reel, 4000	-40 to 125

ESD CAUTION: These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Specifications

1. Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}	PV_{CC}, AV_{CC}	–0.3	30	V
Input voltage, V_I	INPL, INNL, INPR, INNR	–0.3	6.3	V
	PLIMIT, GAIN,	–0.3	GVDD+0.3	V
	MUTE, SD,	–0.3	PVCC+0.3	V
Slew rate, maximum(2)	MUTE, SD		10	V/ms
Operating free-air temperature, T_A		–40	85	°C
Operating junction temperature , T_J		–40	150	°C
Storage temperature, T_{stg}		–40	125	°C
Lead Temperature (Soldering, 10s)			260	°C

(1) Stresses beyond those listed under absolute maximum ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) 100-kΩ series resistor is required if maximum slew rate is exceeded.

2. ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)	±2000	V
		Charged-device model (CDM)	±500	

3. Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	PV_{CC}, AV_{CC}	5		26	V
V_{IH}	High-level input voltage	MUTE, SD	2			V
V_{IL}	Low-level input voltage	MUTE,SD			0.8	V
V_{OL}	Low-level output voltage	FAULTZ, $R_{PULL-UP}$ = 100 kΩ, PV_{CC} = 26 V			0.8	V
I_{IH}	High-level input current	MUTE, SD (V_I = 2 V, V_{CC} = 18 V)			50	μA
R_L(BTL)	Minimum load Impedance	Output filter: L = 10 μH, C = 680 nF	3.2	4		Ω
R_L(PBTL)		Output filter: L = 10 μH, C = 1 μF	1.6	2		
L_o	Output-filter Inductance	Minimum output filter inductance under short-circuit condition	1			μH

4. Thermal Information

THERMAL METRIC		AXS2045 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.8	°C/W

For the PCB layout, see the AXS2045EVM user guide.

5. DC Electrical Characteristics

T_A = 25°C, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 4 Ω, f_s = 400 kHz, hybrid mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V		1.5	5	mV
I_{CC}	Quiescent supply current	SD = 2 V, With load and filter, PV_{CC} = 12 V		12		mA
		SD = 2 V, With load and filter, PV_{CC} = 24 V		18		
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SD = 0.8 V, With load and filter, PV_{CC} = 12 V		20		µA
		SD= 0.8 V, With load and filter, PV_{CC} = 24 V		30		
$r_{DS(on)}$	Drain-source on-state resistance, measured pin to pin	PV_{CC} = 21 V, I_{out} = 500 mA, T_J = 25°C		90		mΩ
G	Gain (BTL)	R1 = 5.6 kΩ, R2 = Open	19	20	21	dB
		R1 = 20 kΩ, R2 = 100 kΩ	25	26	27	
		R1 = 39 kΩ, R2 = 100 kΩ	31	32	33	
G	Gain	R1 = 51 kΩ, R2 = 51 kΩ	19	20	21	dB
		R1 = 75 kΩ, R2 = 47 kΩ	25	26	27	
		R1 = 100 kΩ, R2 = 39 kΩ	31	32	33	
t_{on}	Turn-on time	SD = 2 V		40		ms
t_{OFF}	Turn-off time	SD = 0.8 V		2		µs
GVDD	Gate drive supply	I_{GVDD} < 200 µA	5.1	5.6	6.3	V
V_O	Output voltage maximum under PLIMIT control	$V_{(PLIMIT)}$ = 2 V; V_I = 1 V_{rms}	6.75	8.2	8.75	V

6. AC Electrical Characteristics

T_A = 25°C, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 4 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
KSVR	Power supply ripple rejection	200 mV_{PP} ripple at 1 kHz, Gain = 26 dB, Inputs AC-coupled to GND		–70		dB
P_O	Continuous output power	THD+N = 10%, f = 1 kHz, PV_{CC} = 14.4 V		25		W
		THD+N = 10%, f = 1 kHz, PV_{CC} = 21 V		50		
THD+N	Total harmonic distortion + noise	V_{CC} = 21 V, f = 1 kHz, P_O = 15 W (half-power)		0.1%		
Vn	Output integrated noise	20 Hz to 22 kHz, A-weighted filter,		100		µV
		Gain = 20 dB		–78		dBV
	Crosstalk	V_O = 1 V_{rms}, Gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
Thermal trip point				≥150		°C
Thermal hysteresis				15		°C
Over current trip point				7.5		A

7. Typical Characteristics

f_s = 400 kHz (unless otherwise noted)

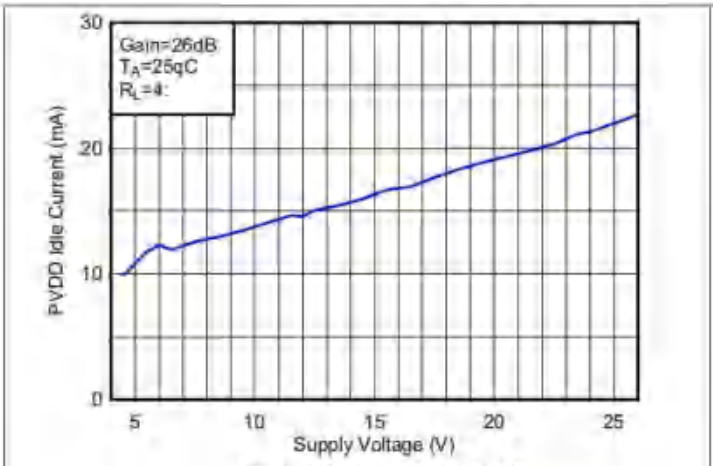


图 1. Idle Current vs PVCC

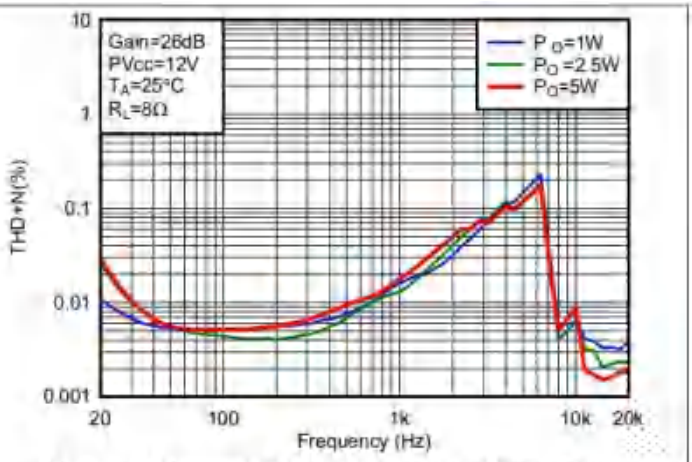


图 2. Total Harmonic Distortion + Noise (BTL) vs Frequency

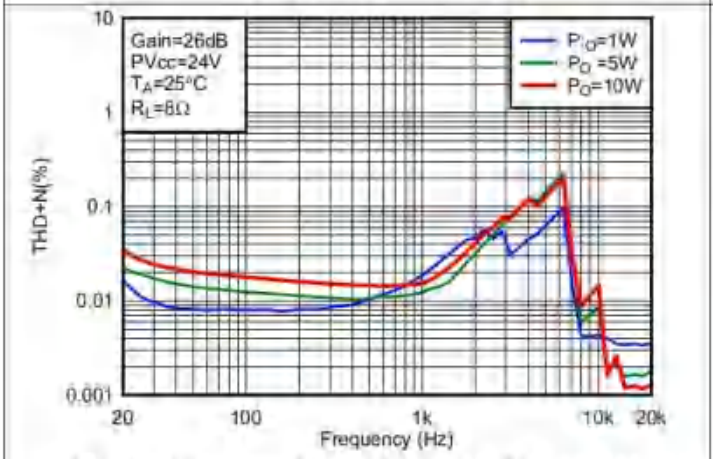


图 3. Total Harmonic Distortion + Noise (BTL) vs Frequency

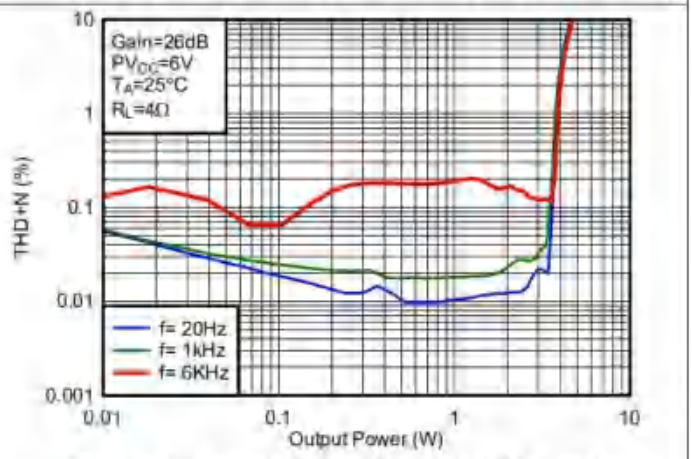


图 4. Total Harmonic Distortion + Noise (BTL) vs Output Power

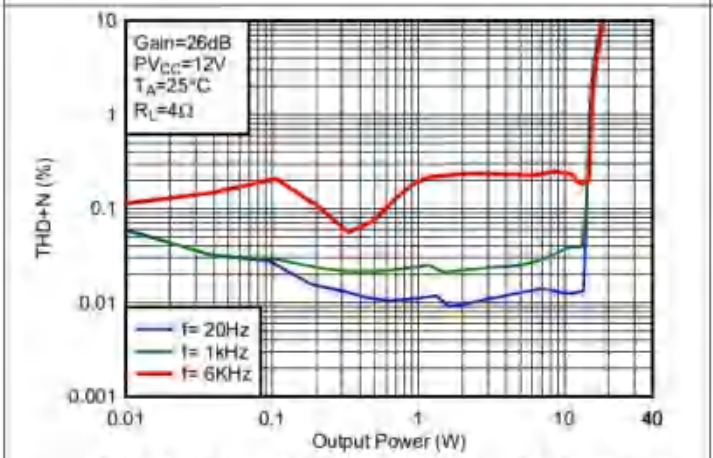


图 5. Total Harmonic Distortion + Noise (BTL) vs Output Power

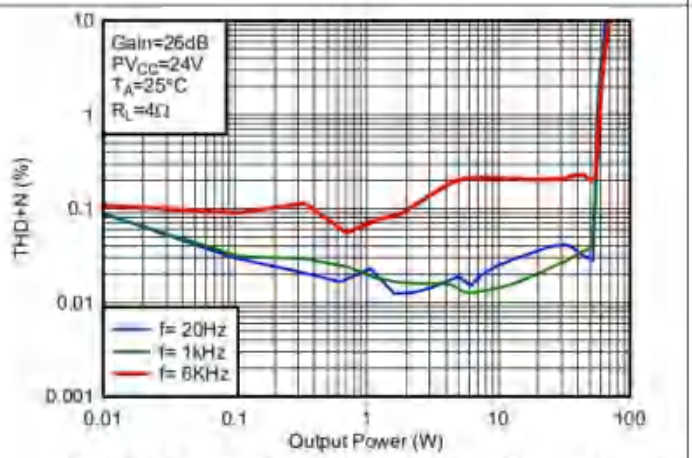


图 6. Total Harmonic Distortion + Noise (BTL) vs Output Power

Typical Characteristics (continued)

f_s = 400 kHz (unless otherwise noted)

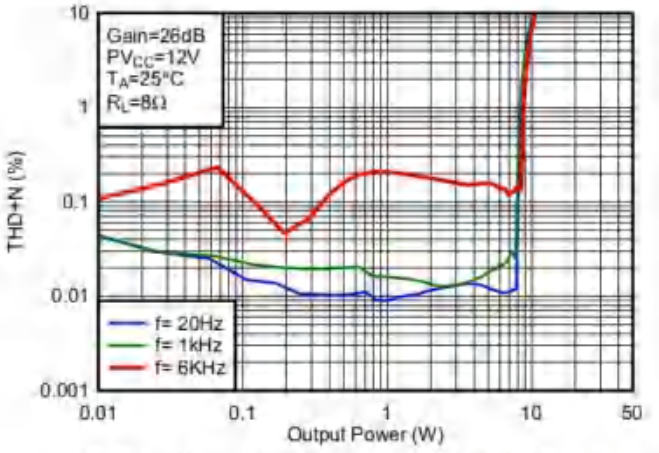


图 7. Total Harmonic Distortion + Noise (BTL) vs Output Power

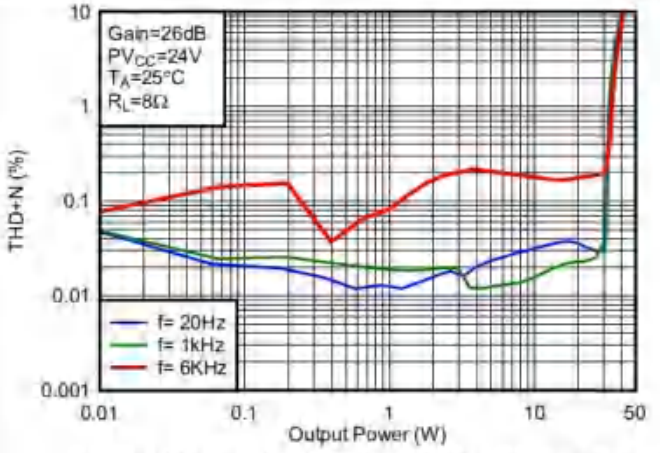


图 8. Total Harmonic Distortion + Noise (BTL) vs Output Power

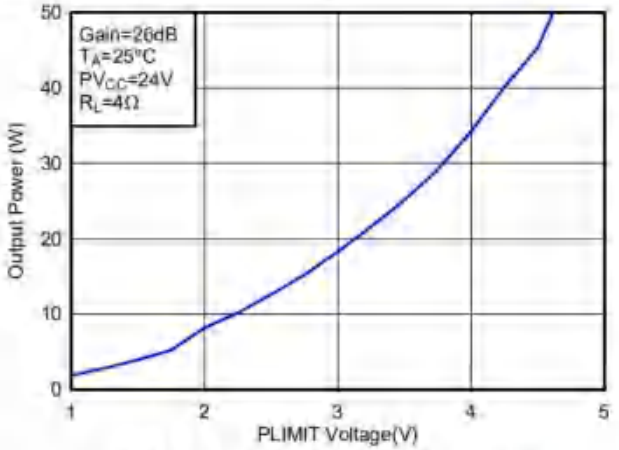


图 9. Output Power (BTL) vs Plimit Voltage

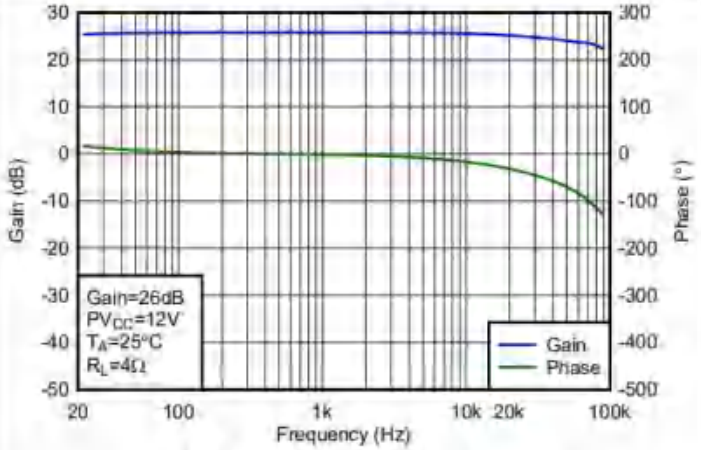


图 10. Gain/Phase (BTL) vs Frequency

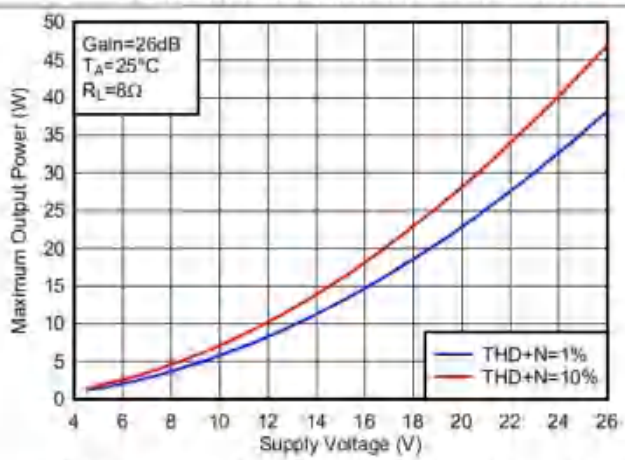


图 11. Maximum Output Power (BTL) vs Supply Voltage

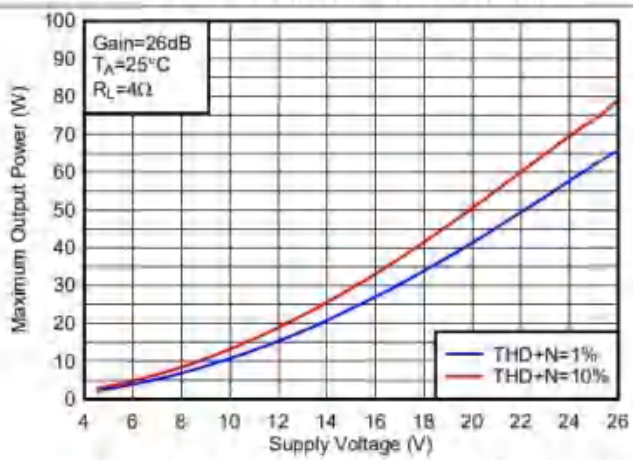


图 12. Maximum Output Power (BTL) vs Supply Voltage

Typical Characteristics (continued)

f_s = 400 kHz (unless otherwise noted)

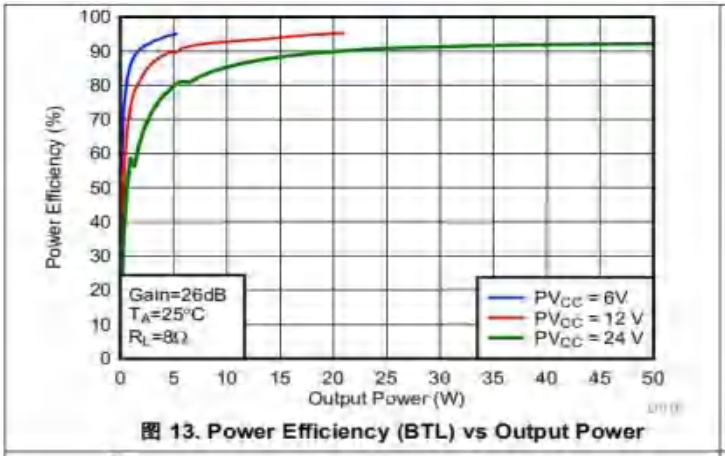


图 13. Power Efficiency (BTL) vs Output Power

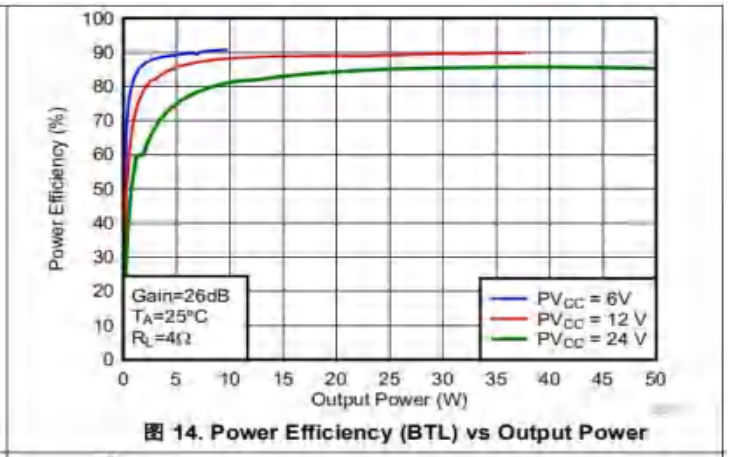


图 14. Power Efficiency (BTL) vs Output Power

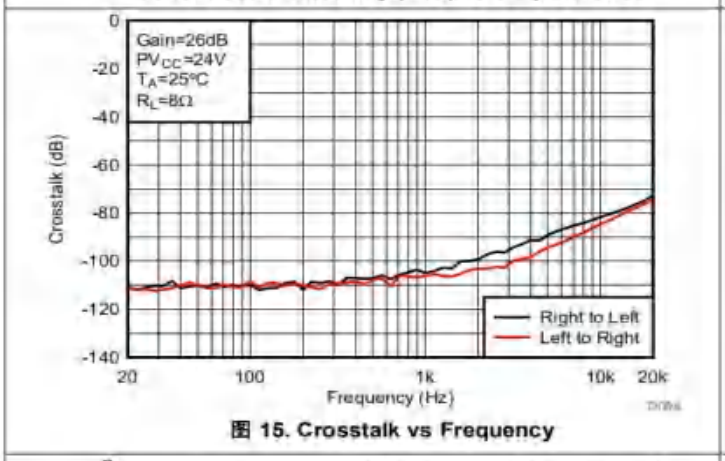


图 15. Crosstalk vs Frequency

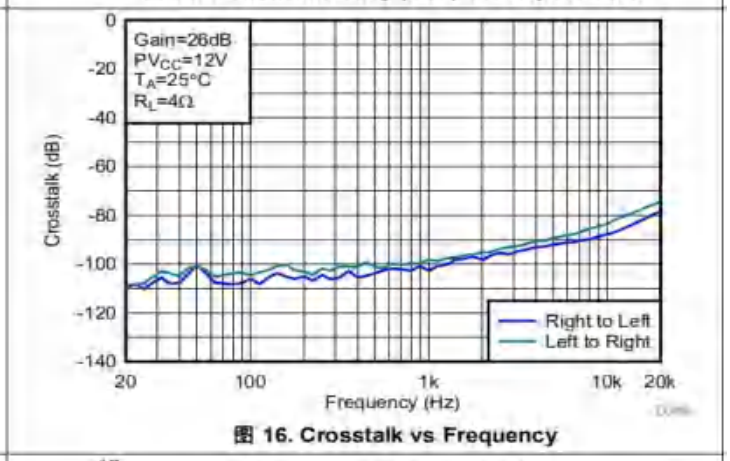


图 16. Crosstalk vs Frequency

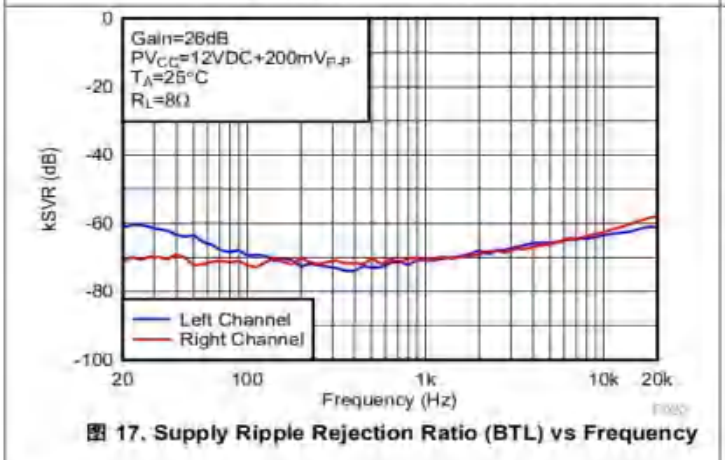


图 17. Supply Ripple Rejection Ratio (BTL) vs Frequency

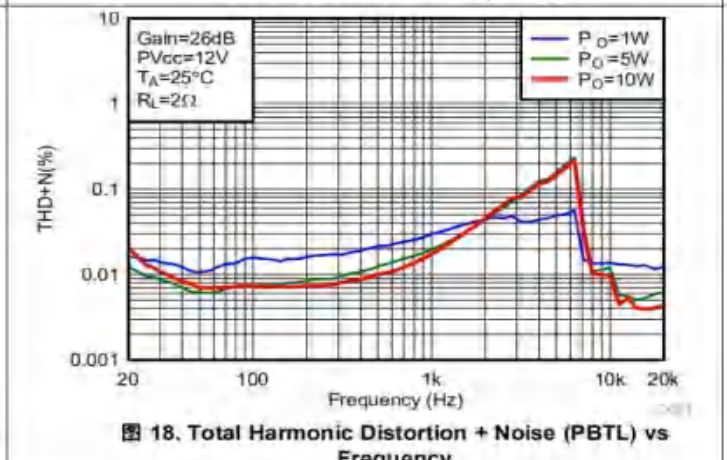


图 18. Total Harmonic Distortion + Noise (PBTL) vs Frequency

Typical Characteristics (continued)

f_s = 400 kHz, (unless otherwise noted)

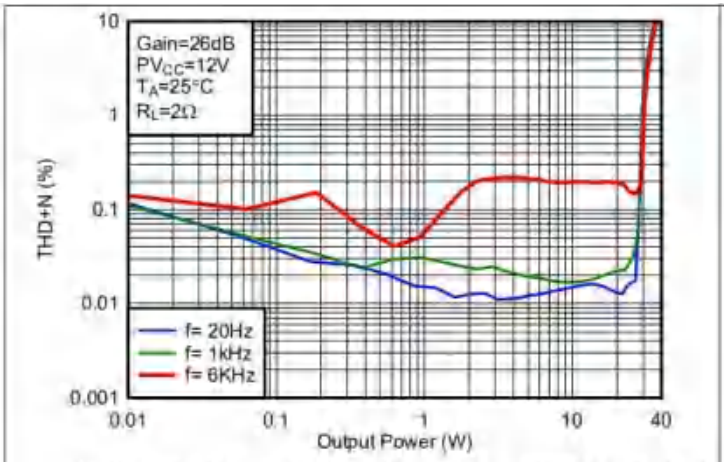


图 19. Total Harmonic Distortion + Noise (PBTL) vs Output Power

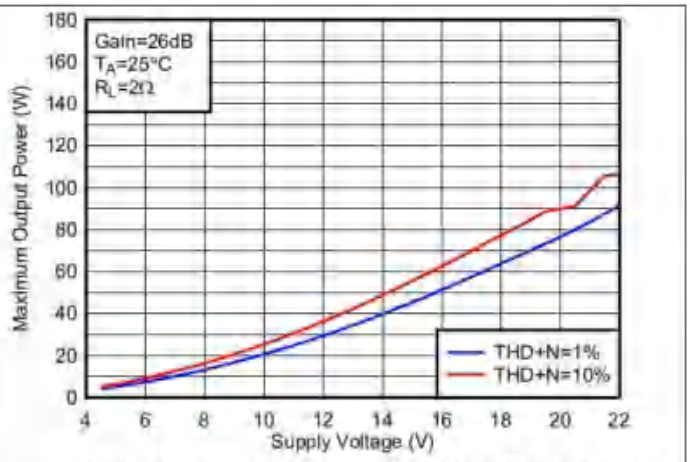


图 20. Maximum Output Power (PBTL) vs Supply Voltage

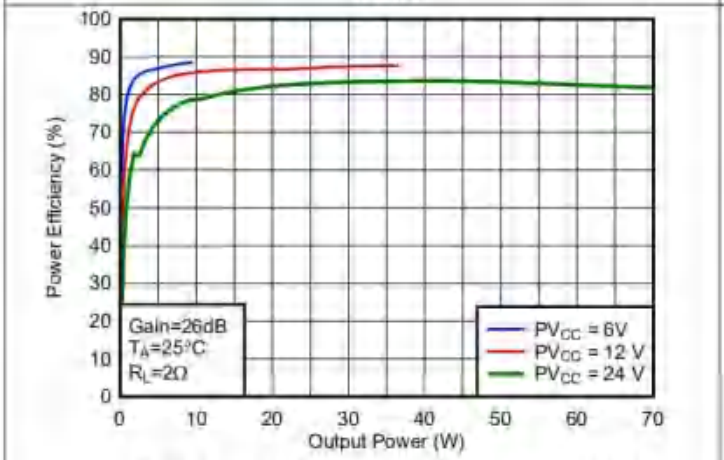


图 21. Power Efficiency (PBTL) vs Output Power

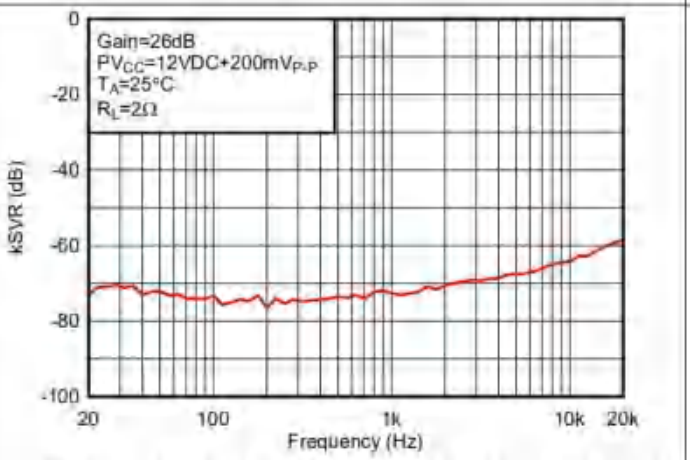


图 22. Supply Ripple Rejection Ratio (PBTL) vs Frequency

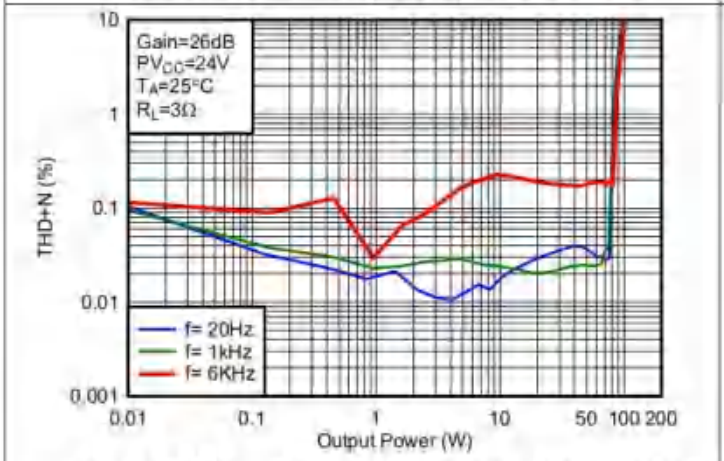


图 23. Total Harmonic Distortion + Noise (PBTL) vs Output Power

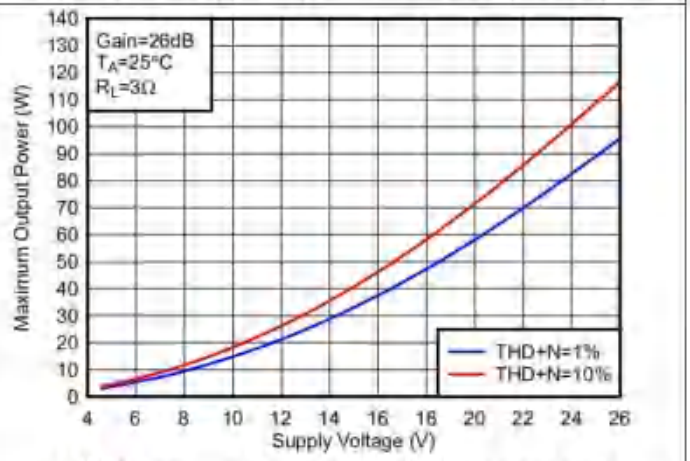


图 24. Maximum Output Power (PBTL) vs Supply Voltage

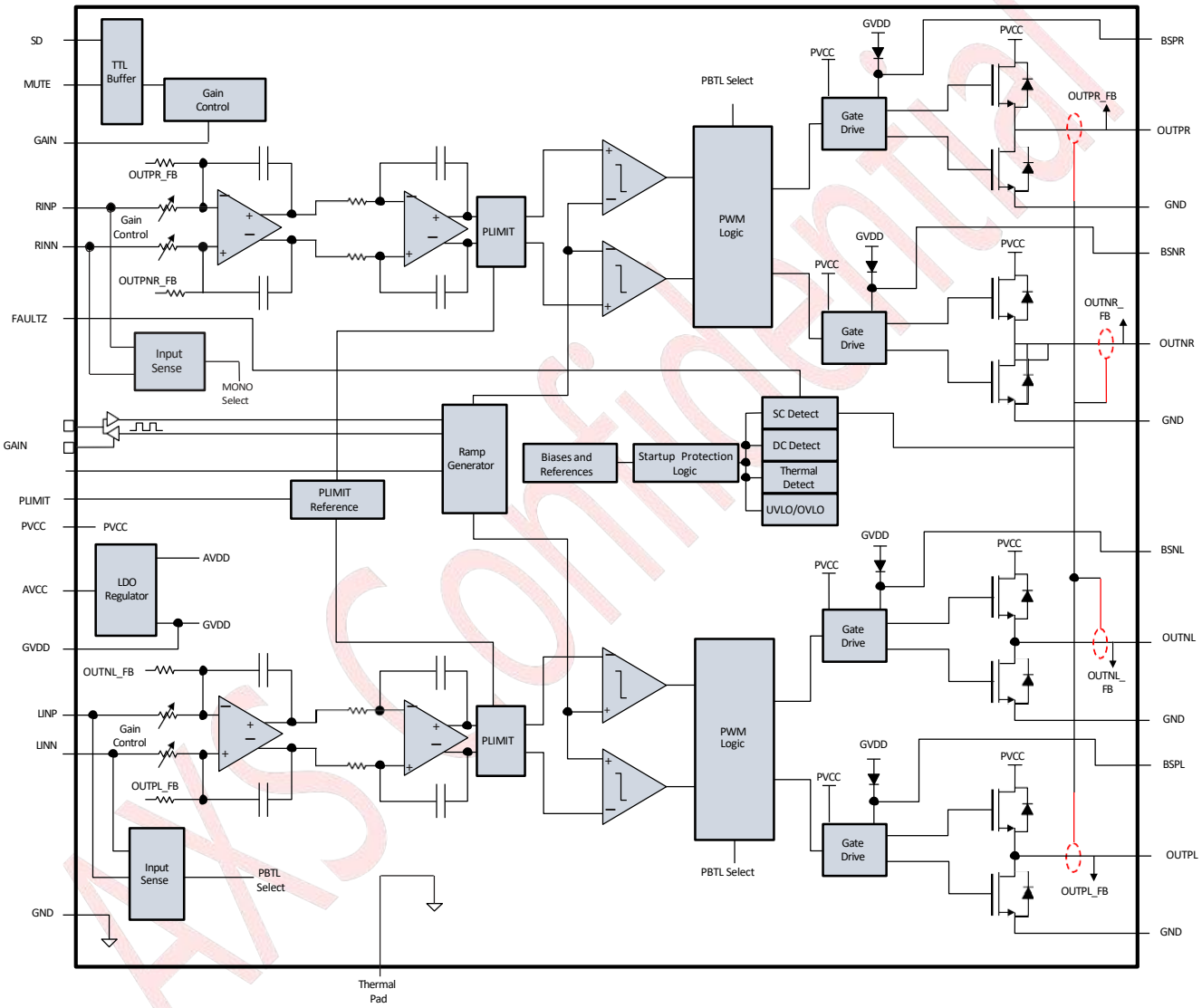
8. Detailed Description

8.1 Overview

The AXS2045 device is a highly efficient Class D audio amplifier with integrated 90m Ohms MOSFET.

The device supports both stereo and mono BTL modes, as well as mono PBTL mode.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Gain Setting

The gain of the AXS2045 is set by the voltage divider connected to the GAIN control pin. An internal ADC is used to detect the input states. The gain setting is latched during power-up and cannot be changed while the device is powered on.

表 1 lists the recommended resistor values for different state settings.

表**1. Gain** Setting

GAIN	R1 (to GND)(1)	R2 (to GVDD)(1)	INPUT IMPEDANCE
20 dB	5.6 kΩ	OPEN	60 kΩ
26 dB	20 kΩ	100 kΩ	30 kΩ
32 dB	39 kΩ	100 kΩ	15 kΩ

(1) Resistor tolerance should be 5% or better.

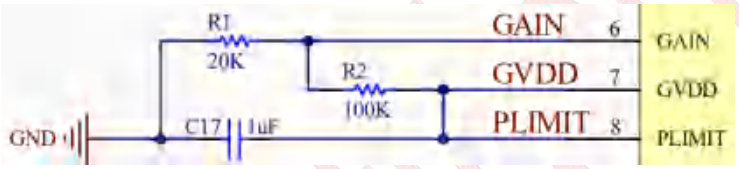


图 **25. Gain Setting**

8.3.2 Input Impedance

The AXS2045 input stage is a fully differential input stage and the input impedance changes with the gain setting from 12.5 kΩ at 32 dB gain to 50 kΩ at 20 dB gain.

表 1 lists the values from min to max gain. The tolerance of the input resistor value is ±20% so that the minimum value will be higher than 5.9 kΩ. The inputs must be AC-coupled to minimize the output DC-offset and ensure correct ramping of the output voltages during power-ON and power-OFF. The input AC-coupling capacitor along with the input impedance forms a high-pass filter with the following cut-off frequency:

$$f = \frac{1}{2\pi Z_I C_x}$$

If a flat bass response is required down to 20 Hz the recommended cut-off frequency is a tenth of that,

2 Hz. 表 2 lists the recommended AC-coupling capacitors for each gain setting. If a –3-dB frequency response is accepted at 20 Hz, 10 times lower capacitors (for example, a 1-µF capacitor) can be used.

表**2. Recommended Input AC-Coupling Capacitors**

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	50 kΩ	1.5 µF	2.1 Hz
26 dB	25 kΩ	3.3 µF	1.9 Hz
32 dB	12.5 kΩ	5.6 µF	2.3 Hz

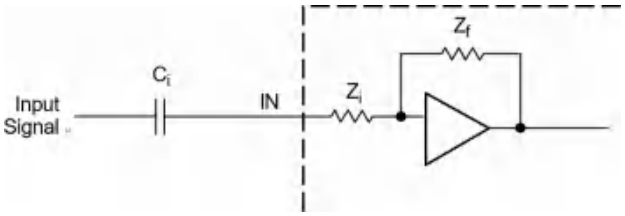


图 **26. Input Impedance**

The input capacitors should be a type of low leakage, such as quality electrolytic, tantalum, or ceramic caacitors. If a polarized type is used the positive connection should face the input pins which are biased to 3 Vdc.

8.3.3 Startup and Shutdown Operation

The AXS2045 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of non-use for power conservation.

The SDZ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling SDZ low puts the outputs to mute and the amplifier to enter a low-current state. Do not leave SDZ unconnected, because the amplifier operation is unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply. The gain setting is selected at the end of the start-up cycle, and cannot be changed until the next power- up.

8.3.4 PLIMIT Operation

The AXS2045 has a built-in voltage limiter that can be used to limit the output voltage level below the supply rail. The amplifier operates as if it was powered by a lower supply voltage, and thereby, limits the output power. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin.

An external reference may also be used if tighter tolerance is required. Add a 1-µF capacitor from pin PLIMIT to ground to ensure stability.

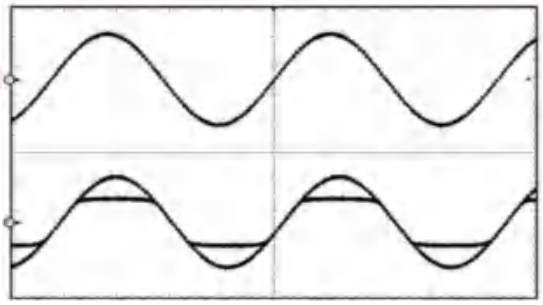


图**27. Power Limit Example**

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. This is done by limiting the duty cycle to a fixed maximum value. The limit can be considered as a "virtual" voltage rail which is lower than the supply connected to PVCC. The "virtual" rail is approximately four times the voltage at the PLIMIT pin.

The output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power}$$

where

- P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)
- R_L is the load resistance.
- R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.
- V_P is the peak amplitude, which is limited by the "virtual" voltage rail.

表**3. Power Limit Example**

PV_{CC} (V)	PLIMIT VOLTAGE (V)(1)	R to GND	R to GVDD	OUTPUT VOLTAGE (V_{rms})
24 V	GVDD	Open	Short	17.9
24 V	3.3	45 kΩ	51 kΩ	12.67
24 V	2.25	24 kΩ	51 kΩ	9
12 V	GVDD	Open	Short	10.33
12 V	2.25	24 kΩ	51 kΩ	9
12 V	1.5	18 kΩ	68 kΩ	6.3

PLIMIT measurements taken with EVM gain set to 26 dB and input voltage set to 1 V_{rms}.

8.3.5 GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. The GVDD supply can also be used to supply the PLIMIT and GAIN voltage dividers. Decouple GVDD with a X5R ceramic 1-µF capacitor to GND. The GVDD supply is not intended to be used for external supply.

The current consumption should be limited by using resistor voltage dividers for GAIN and PLIMIT of 100 kΩ or more.

8.3.6 BSPx and BSNx Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-nF ceramic capacitor of quality X5R or better, rated for at least 16 V, must be connected from each output to the corresponding bootstrap input. (See the application circuit diagram in 图 32.)

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

8.3.7 Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the AXS2045 with a differential source, connect the positive lead of the audio source to the RINP or LINP input and the negative lead from the audio source to the RINN or LINN input.

To use the AXS2045 with a single-ended source, AC ground the negative input through a capacitor equal in value to the input capacitor on positive and apply the audio source to either input. In a single-ended input application, the unused input should be AC grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible to allow the input DC blocking capacitors to become completely charged during the 40-ms power-up time. If the input capacitors are not allowed to completely charged, there will be some additional sensitivity to the component matching which can result in pop if the input components are not well matched.

8.3.8 Device Protection System

The AXS2045 contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against any kind of permanent failures due to short circuits, overload, over temperature, and under-voltage.

The FAULTZ pin signals if an error is detected according to 表 4:

表**4. Fault Reporting**

FAULT	TRIGGERING CONDITION (typical value)	FAULTZ	ACTION	LATCHED /SELF-LEARING
Over Current	Output short or short to PVCC or GND	Low	Output high impedance	Latched
Over Temperature	T_j > 150°C	Low	Output high impedance	Latched
Too High DC Offset	DC output voltage	Low	Output high impedance	Latched
Under Voltage on PVCC	PVCC < 4.5V	–	Output high impedance	Self-clearing
Over Voltage on PVCC	PVCC > 27V	–	Output high impedance	Self-clearing

8.3.9 DC Detect Protection

The AXS2045 has circuitry which protects the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault is reported on the FAULT pin as a low state. The DC Detect fault causes the amplifier to shutdown by changing the state of the outputs to Hi-Z.

If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. Connecting the FAULTZ and SDZ pins allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the DC Detect protection latch.

A DC Detect Fault is issued when the output differential voltage of either channel exceeds DC protection threshold level for more than 640 ms at the same polarity.

表 5 shows some examples of the typical DC Detect Protection threshold for several values of the supply voltage. The Detect Protection Threshold feature protects the speaker from large DC currents or AC currents less than 2 Hz. To avoid nuisance faults due to the DC detect circuit, hold the SD pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

表 5 lists the minimum output offset voltages required to trigger the DC detect. The outputs must remain at or above the voltage listed in the table for more than 640 ms to trigger the DC detect.

表**5. DC Detect Threshold**

PV_{CC} (V)	V_{OS} - OUTPUT OFFSET VOLTAGE (V)
4.5	1.35
6	1.8
12	3.6
18	5.4

8.3.10 Short-Circuit Protection and Automatic Recovery Feature

The AXS2045 has protection from over current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the FAULTZ pin as a low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SDZ pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. Connecting the FAULTZ and SDZ pins allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the short-circuit protection latch.

8.3.11 Thermal Protection

Thermal protection on the AXS2045 prevents damage to the device when the internal die temperature exceeds 150°C. This trip point has a ±15°C tolerance from device to device. Once the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are disabled. This is a latched fault. Thermal protection faults are reported on the FAULTZ terminal as a low state.

If automatic recovery from the thermal protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the thermal protection latch.

8.3.12 Device Modulation Scheme

The AXS2050 is internally fixed to BD mode for better performance. This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker.

The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages.

The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current,

which reduces any I^2R losses in the load.

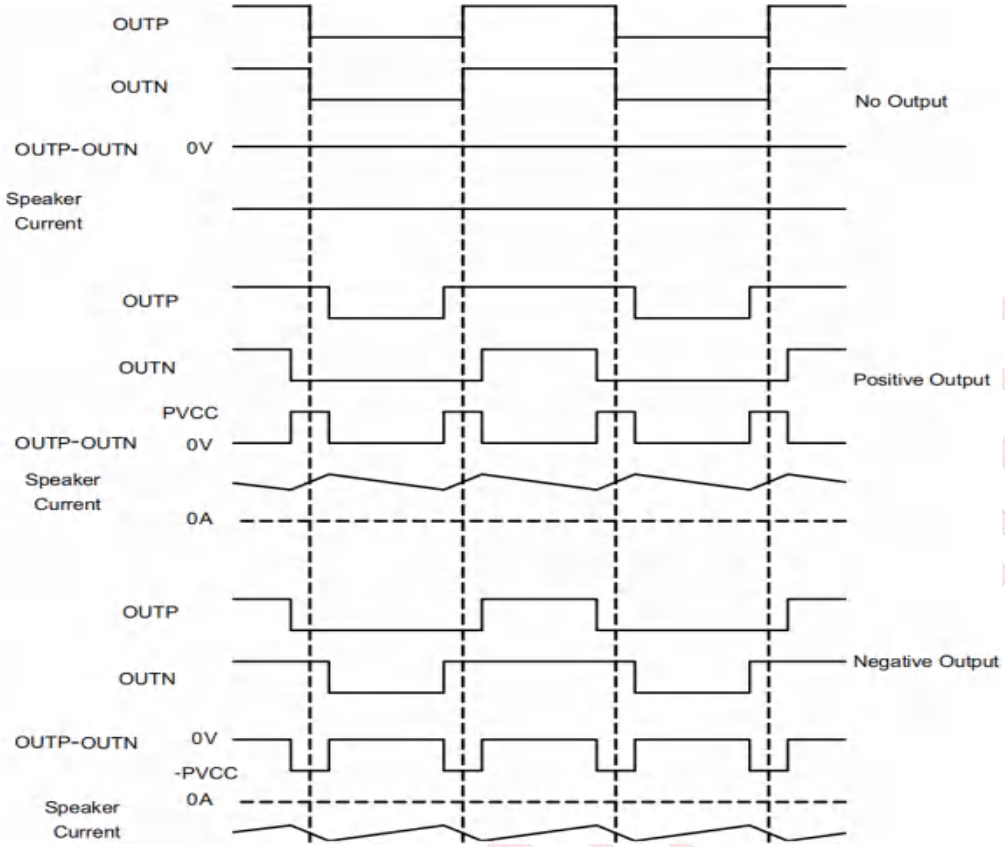


图28. BD Mode Modulation

8.3.13 Efficiency: LC Filter Required with the Traditional Class-D Modulation Scheme

The AXS2045 modulation schemes have little loss in the load without a filter because the pulses are short and the change in voltage is VCC instead of 2 × VCC. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not required. An LC filter with a cut off frequency less than the class-D switching frequency allows the switching current to flowthrough the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

8.3.14 Ferrite Bead Filter Considerations

Using the Advanced Emissions Suppression Technology in the AXS2045, a high efficiency Class-D audio amplifier can be designed while minimizing interference to the surrounding circuits. Designing the amplifier can also be accomplished with only a low-cost ferrite bead filter. In this case the user must carefully select the ferrite bead used in the filter. One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, therefore the user must select a material that is effective in the 10-MHz to 100-MHz range which is key to the operation of the Class-D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30-MHz. The ferrite bead filter should be used to block radiation in the 30-MHz and above range from appearing on

the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000-pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead or capacitor filter should be less than 10-MHz.

Also, the ferrite bead must be large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, the device can also estimate the bead current handling capability by measuring the resonant frequency of the filter output at low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable.

A high quality ceramic capacitor is also required for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the Class-D outputs to ground. Suggested values for a simple RC series snubber network would be 18-Ω in series with a 330-pF capacitor, although design of the snubber network is specific to different applications and must be designed with the consideration of the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, verify the layout of the snubber network is tight and returns directly to the GND pins on the IC.

8.3.15 When to Use an Output Filter for EMI Suppression

A complete LC reconstruction filter should be added in some circuit instances. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases, a classic second order Butterworth filter similar to those shown in 图 29 can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, LC reconstruction filters can be the lowest-cost methods to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective in preventing line conducted interference.

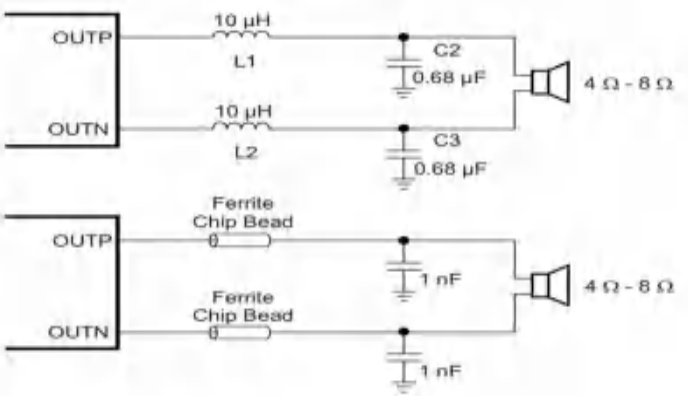


图**29. Output Filters**

9. Device Functional Modes

9.1 Mono PBTL Mode

AXS2045 can be configured in mono PBTL mode, the device can deliver up to 60-W output power.

- Connect LINP and LINN directly to Ground (without capacitors), so the device is set in a mono PBTL mode during power up.
- Connect OUTPR and OUTNR together for the positive speaker terminal, and OUTNL and OUTPL together for the negative speaker terminal.
- Analog input signal is applied to RINP and RINN.

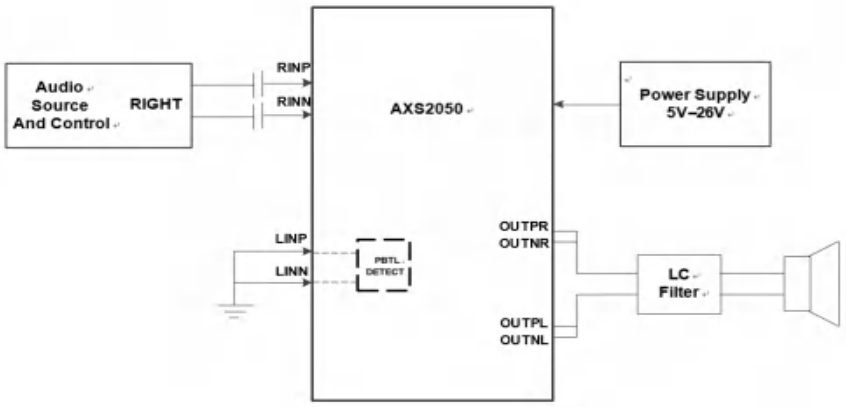


图 **30 Mono PBTL Mode**

9.2 Mono BTL Mode (Single Channel Mode)

The AXS2045 can be connected in mono BTL mode while cutting the idle power-loss nearly by half.

- Connect RINP and RINN directly to Ground (without capacitors), so the device is set in mono BTL mode during power up.
- Connect OUTPL to the positive speaker terminal, and OUTNL to the negative speaker terminal.
- Analog input signal is applied to LINP and LINN.

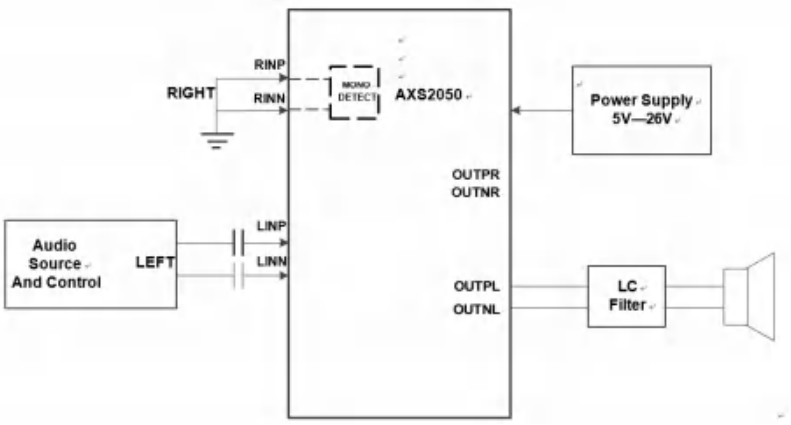


图**31. Mono BTL Mode**

10. Application Information

10.1 Typical Application

The AXS2045 is configured as stereo BTL outputs with no power limit implemented.

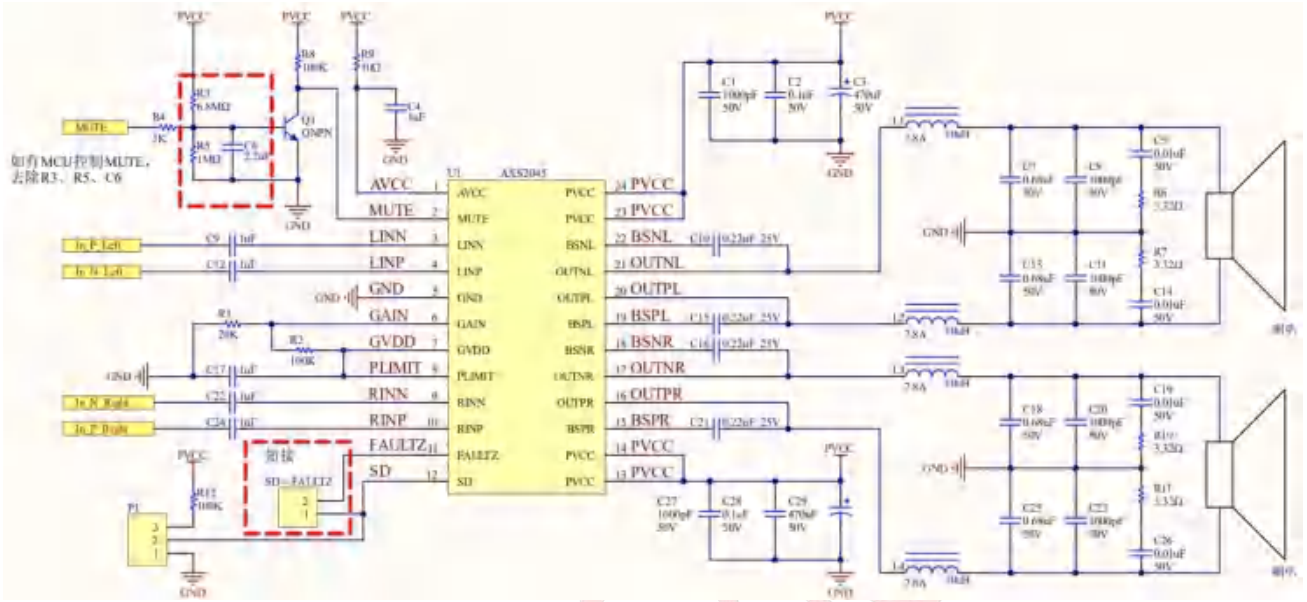


图32. AXS2045 Typical Schematic

10. 2 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range PVCC	5 V to 26 V
Maximum output power	2 × 30 W

10.3 Detailed Design Procedure

The AXS2045 devices are very flexible and easy-to-use Class D amplifiers; therefore, the design process is straightforward. Before beginning the design, gather the following information regarding the audiosystem.

- PVCC rail planned for the design
- Speaker or load impedance
- Maximum output power requirement
- Desired PWM frequency

10.3.1 Select the Amplifier Gain

To select the amplifier gain setting, the designer must determine the maximum power target and the speaker impedance. Once these parameters have been determined, calculate the required output voltage swing which delivers the maximum output power. Choose the lowest analog gain setting that corresponds to produce an output voltage swing greater than the required output swing for maximum power. The analog gain can be set by selecting the voltage divider resistors (R1 and R2) on the Gain pin.

10.3.2 Select Input Capacitance

Select the bulk capacitors at the PVCC inputs for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well-designed power supply, two 220μF/50V capacitors should be sufficient. One capacitor should be placed near the PVCC inputs at each side of the device. PVCC capacitors should be a low ESR type because they are being used in a fast-switching application.

10.3.3 Select Decoupling Capacitors

Good quality decoupling capacitors must be added at each of the PVCC inputs to provide good reliability, good audio performance, and to meet regulatory requirements. X5R or better ratings should be used in this application. Consider temperature, ripple current, and voltage overshoots when selecting decoupling capacitors. Also, these decoupling capacitors should be located near the PVCC and GND connections to the device in order to minimize series inductances.

10.3.4 Select Bootstrap Capacitors

Each of the outputs require bootstrap capacitors to provide gate drive for the high-side output FETs. For this design, use 0.22-μF, 25-V capacitors of X5R quality or better.

10.3.5 Power Supply Recommendations

The AXS2045 device requires an external power supply, between 5 V and 26 V, for the analog circuitry (AVCC) and the power stage (PVCC) of the amplifier. Several on-chip regulators are included on the AXS2045 to generate the voltages necessary for the internal circuitry of the audio path. The voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. The AVCC supply feeds internal LDO including GVDD. This LDO output are connected to external pins for filtering purposes, but should not be connected to external circuits. GVDD LDO output have been sized to provide current necessary for internal functions but not for external loading.

10.3.6 Power Supply Mode

The AXS2045 supports both single and dual power supply modes. For dual power supply mode application, when AVCC is supplied with 5V power, PVCC is recommended to be lower than 20 V. When PVCC is supplied with power greater than 20 V, AVCC is recommended to be higher than 6 V.

10.3.7 Layout Guidelines

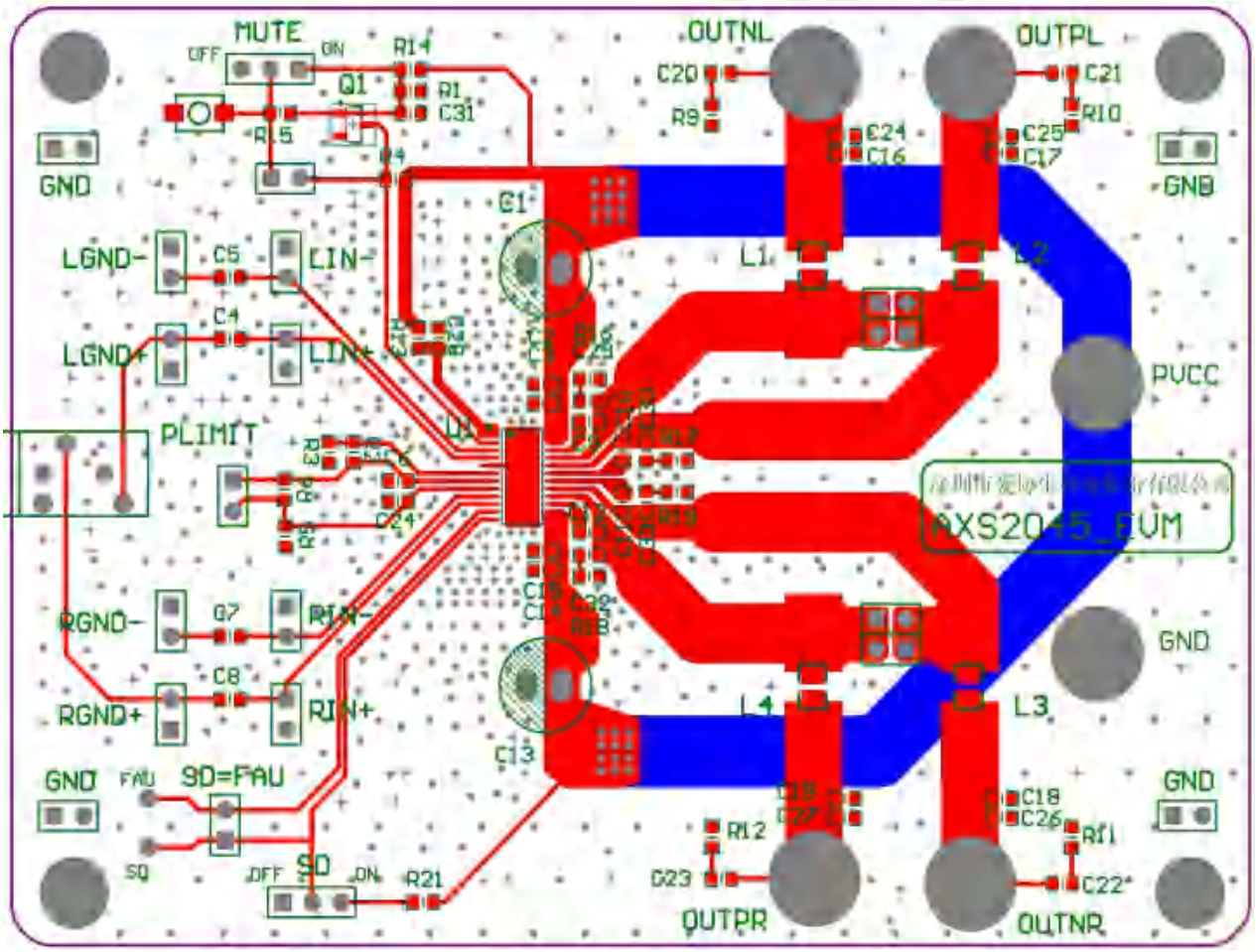
The AXS2045 can be used with a small, inexpensive ferrite bead output filter in most applications. However, because the Class-D switching edges are fast, the layout of the printed circuit board must be planned carefully. The following suggestions helps to meet EMC requirements.

- Decoupling capacitors — The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (220-μF or greater) bulk power supply

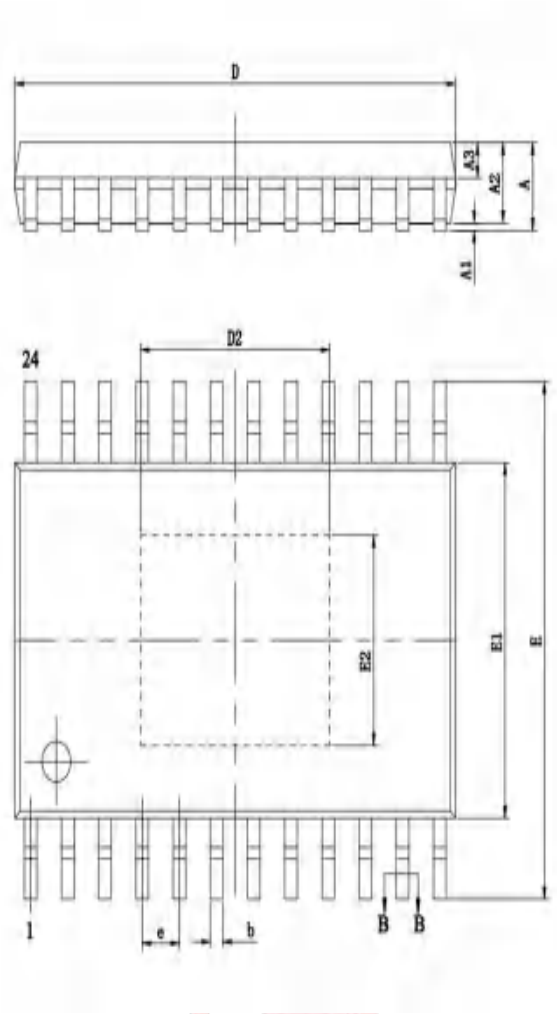
decoupling capacitors should be placed near the AXS2045 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the IC GND pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220-pF and 1-nF, and a larger mid-frequency cap of value between 100-nF and 1-µF also of good quality to the PVCC connections at each end of the chip.

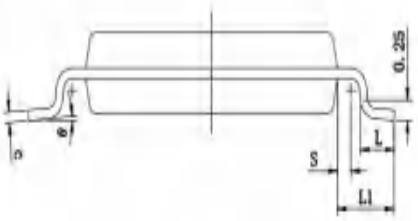
- Minimize the current loop from each of the outputs through the ferrite bead filter and back to GND. The size of this current loop determines its effectiveness as an antenna.
- Grounding — The PVCC decoupling capacitors should connect to GND. All ground should be connected at the IC GND, which should be used as a central ground connection or star ground for the AXS2045.
- Output filter — The ferrite EMI filter should be placed as close to the output terminals as possible for the best EMI performance. The LC filter should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded.

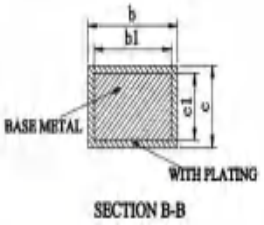
10.3.8 Layout Example



封装图（ETSSOP24）







SECTION B-B

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

L/F载体尺寸 (mil)	E2	D2
122*190	2.75~2.95	4.73~4.93

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